AMENDMENTS TO THE SPECIFICATION:

Please replace the title beginning on page 1 at line 1 with the following:

RATE N/N QUASI-SYSTEMATIC, RECURSIVE CONVOLUTIONAL ENCODER AND CORRESPONDING DECODER

Please replace the paragraph beginning on page 1 at line 7 with the following:

This invention generally relates to convolutional encoders, and, more specifically, to rate n/n ~~systematic,~~ recursive convolutional encoders for use in serial concatenated coding and serial concatenated trellis coded modulation.

Please replace the paragraph beginning on page 2 at line 7 with the following:

In Narayanan et al., a rate 1 differential encoder is proposed for the inner encoder of a SCTCM encoder. Two successive encoded bits are mapped into symbols using $\pi/4$-DQPSK modulation. The rate 1 differential encoder of Narayanan is illustrated in Figure 1A. Input bits are provided as an input to adder 2 over signal line 1. The output 5 of storage element 3 is also provided as an input to adder 2 over signal line 4. The sum from the adder 2 is stored in storage element 3.

Please replace the paragraph beginning on page 2 at line 20 with the following:

In accordance with one aspect of the invention, there is provided a rate n/n recursive, quasi-systematic convolutional encoder. The encoder has n inputs, n parallel outputs, an adder having (n+1) inputs and an output, n being an integer greater than 1, and a feedback loop, including one or more storage elements in series, from the output of the adder to an input thereof. The feedback loop and the one or more storage elements may be characterized by a prime polynomial. In addition, all n encoder inputs are input to the adder, (n-1) of the encoder inputs are passed through unaltered to form (n-1) of the encoder outputs, and the nth encoder output is derived from the feedback loop.

Please replace the paragraph beginning on page 3 at line 9 with the following:

A method in accordance with the subject invention comprises the steps of inputting n bits to a rate n/n quasi-systematic, recursive convolutional encoder configured in accordance with the invention, wherein n is an integer greater than 1; receiving in parallel from the encoder the resultant n output bits; and mapping the n output bits into a D-dimensional channel symbol, wherein D is an integer of 1 or more, the order of mapping being greater than BPSK. In one implementation, applicable in the case in which D is greater than 1, the method further comprises the step of serializing the D components of the channel symbol, 2 at a time.

Please replace the paragraph beginning on page 5 at line 20 with the following:

A SCCC decoder, illustrated in Figure 1C, is typically iterative. An inner decoder 12 is coupled in series with de-interleaver 13 which in turn is coupled in series with outer decoder 14. A feedback loop is provided between an output of outer decoder 14 and an input of inner decoder 12. Included in the feedback loop is interleaver 16. After transmission over a channel, incoming bits are input to inner decoder 12 over signal line 11. The output of outer decoder 14 is fed back to interleaver 16 over signal line 15. A priori information is provided to the inner decoder 12 from interleaver 16 over signal line 17. After a prescribed number of iterations, the decoded bits are output by the outer decoder on signal line 18.

Please replace the paragraph beginning on page 6 at line 21 with the following:

The polynomial characterizing the feedback loop in Figure 11A can be expressed as follows: $h_0 + (h_1 \times X) + \bullet\bullet\bullet + (h_{r-1} \times X^{r-1}) + (h_r \times X^r)$, in which $h_0=h_r=1$ and h_i, where $0 < i < r$, can be either 0 or 1, depending on the state of modules 63b, 63c. For example, in the case in which r=3, and module 63c [[i]] is such that $h_1=1$, and module 63b is such that $h_2=0$, the polynomial characterizing the feedback loop can be expressed as X^3+X+1.

Please replace the paragraph beginning on page 8 at line 3 with the following:

A first embodiment of a rate 3/3 encoder in accordance with the subject invention is illustrated in Figure 3A. As shown, this encoder comprises 3 inputs, identified with numeral 21, and 3 outputs, identified with numeral 22. Each of the 3 inputs 21a, 21b, 21c is input to adder 24. In addition, two of the inputs, 21a and 21b, are systematic inputs and are passed directly through the encoder to form outputs 22a and 22b. The output of the adder 24 is coupled to storage device 25. The output of storage device 25 forms output 22c. In addition, the output of storage device 25 forms an input to adder 24 over signal line 26.

Please replace the paragraph beginning on page 8 at line 11 with the following:

A second embodiment of a rate 3/3 encoder in accordance with the subject invention is illustrated in Figure 3B. As shown, this encoder comprises 3 inputs, identified with numeral 27, and 3 outputs, identified with numeral 30. Each of the 3 inputs 27a, 27b, 27c is input to adder 28. In addition, two of the inputs, 27a and 27b, are systematic inputs and are passed directly through the encoder to form outputs 30a and 30b. The output of the adder 28 forms output 30c. In addition, the output of adder 28 is fed over signal line 32 as an ~~the~~ input to storage device 31. The output of storage device 31 forms an input to adder 28 over signal line 33 to complete a feedback loop. Compared to the embodiment of Figure 3B, the embodiment of Figure 3A is preferred because it will have slightly better distance distribution properties, although both are advantageous in relation to the prior art.

Please replace the paragraph beginning on page 8 at line 21 with the following:

An embodiment of a rate 2/2 encoder in accordance with the subject invention is illustrated in Figure 4. As shown, the encoder has 2 inputs, identified with numeral 34, and 2 outputs, identified with numeral 35. Each of the two inputs 34a, 34b is input to adder 36. In addition, one of the inputs, 34a, is a systematic input and is passed directly through the encoder to form output 35a. The output of adder 36 forms the input to storage device 37. The output of

storage device 37 forms output 35b. In addition, the output of storage device 37 forms an input to adder 36 over signal line 38.

Please replace the paragraph beginning on page 8 at line 28 with the following:

An embodiment of a rate 4/4 encoder in accordance with the subject invention is illustrated in Figure 5. As shown, this encoder comprises 4 inputs, identified with numeral 39, and 4 outputs, identified with numeral 40. Each of the 4 inputs 39a, 39b, 39c, 39d is input to adder 63. In addition, three of the inputs, 39a, 39b, 39c are systematic inputs and are passed directly through the encoder to form outputs 40a, 40b, 40c. The output of the adder 63 is coupled to storage element 42. The output of storage element 42 forms output 40d. In addition, the output of storage element 42 forms an input to adder 63 over signal line 43.

Please replace the paragraph beginning on page 9 at line 7 with the following:

The rate n/n encoder of the subject invention may comprise or form part of an inner encoder of a SCCC or SCTCM encoder. Figure 6 illustrates an inner encoder for a SCTCM encoder which incorporates the rate n/n encoder of the subject invention. As illustrated, the inner encoder comprises a serial to parallel (S/P) converter 44, a rate n/n encoder 45 configured in accordance with the subject invention, a bit to symbol mapper 46, and, optionally, a symbol multiplexor 47. Incoming bits (such as from interleaver 8 in Figure 1B) 48 are serially input to S/P converter 44. S/P converter 44 converts the serial stream of input bits to successive parallel renditions of n bits each. Each n bit rendition 50 is input to a rate n/n encoder 45 configured in accordance with the subject invention. The output of the rate n/n encoder comprises successive parallel renditions of n bits each. Each n bit rendition 51 is input to bit to symbol mapper 46. Bit to symbol mapper 46 converts each rendition 51 of n bits to a D-dimensional channel symbol, where D is an integer equal to 1 or more. In the case in which n=D=1, the symbol multiplexor 47 is unnecessary. In the cases in which n ~~≠~~D or n=D>1, the symbol multiplexor 47 ~~serialize~~serializes the D components 52 of a D-dimensional symbol and outputs the same on

signal line 49. In one implementation, the multiplexor serializes the D components 2 at a time to represent the I and Q components of a quadrature output.

Please replace the paragraph beginning on page 12 at line 6 with the following:

Figure ~~11~~10 is a flowchart illustrating an embodiment of a method of operation in accordance with the subject invention. In step 52, an n-tuple of bits is input to a rate n/n encoder configured in accordance with the subject invention, where n is an integer greater than 1. In step 53, an n-tuple of bits is received as an output from the encoder. In step 54, the n-tuple of output bits is mapped into a D-dimensional channel symbol, where D is an integer greater than or equal to 1. In one implementation, a Gray mapping is employed in which the tuple of bits corresponding to adjacent symbols differ by no more than 1 bit.

Please replace the paragraph beginning on page 16 at line 15 with the following:

In step ~~133~~127, the a priori C input to the inner SISO 115 is subtracted from these LLRs to form extrinsic information output from the U output of inner SISO 115.

Please replace the paragraph beginning on page 16 at line 17 with the following:

In step ~~127~~128, after passage through de-interleaver 16, these values are provided as a priori information to the C input of outer SISO 117. Responsive thereto, in step ~~128~~129, the outer SISO 117 computes the LLRs for each of the coded bits c_n.

Please replace the paragraph beginning on page 16 at line 20 with the following:

In step ~~134~~130, the a priori information provided to the C input of outer SISO 117 is subtracted from these LLRs to provide extrinsic information.

Please replace the paragraph beginning on page 16 at line 22 with the following:

In step ~~129~~131, after passage through interleaver 118, these extrinsic values are provided as a priori information to the U input of inner SISO 115.

Please replace the paragraph beginning on page 16 at line 24 with the following:

In decision block ~~130~~132, it is determined whether additional iterations should be performed. If so, the process is repeated, beginning with step 126. If not, a jump is made to step ~~131~~133. In step ~~131~~133, in the outer SISO 117, the LLR for each unencoded bit d_k is determined, and then, in step ~~132~~134, the LLRs are compared with a predetermined threshold to determine estimates of the unencoded bits d_k.

Please replace the paragraph beginning on page 25 at line 3 with the following:

A rate n/n recursive, quasi-systematic encoder. In combination with a bit to symbol mapper, the encoder advantageously forms an inner encoder of a serial concatenated trellis coded modulation encoder. The encoder may also form the inner encoder of a serial concatenated convolutional encoder. A related decoder is also described.